The Adaptive System **2D** of Processing and Visualization of a Real-time. **The Electron Conveyor.**

The Adaptive System 2D of Real-time Processing and Visualization is not rigid, and is structured as a designer set consisting of sets of modules performing elementary mathematical and logical functions and integrated in the processing conveyor based as CAD systems.

The circuitry of the **Adaptive System 2D Real-time Processing and Visualization** consists of a set of Functional Elements - FE, built to the generalized standard of graphics information processing - ***File-VideoFrame*** - **FVF**. Each FE **FVF** can be: an independent frame, part of poly-monitor system, part of the polyscreen system, a frame or series of frames of cine, part of RAM of the specialized processor for data/image processing.

The software is used to initiate available FE of Adaptive System, sets FE parameters, organizes data transfer and controls dynamic processes. The hardware automatically implements structure of software configured stream conveyor and is also launched by running software.

FE of designer systems represents an electron hardware with limited set of statuses depending on different levels of complexity that are set by ***Adaptive Management System*** and, afterwards, FE performs independent tasks until new parameters are configured.
The statuses of FE can be both static and dynamic. The change of FE statuses is set in a period between frames.
In order to ensure parallel data input, processing and output (any operation may deal with different formats) each FVF is adapted to sync line/frame memory addressing to static frame memory.
Addressing Frame Synchronization - **FrmSynch** performs simultaneous frames management and represents as the Synchronous Generator as a specialized FE -.

The control procedures for FE are carried out through special bus - universal for all FE: - Status and Configuration Control bus - ***Configuration BUS*** - **ConfgBUS**.
At initialization of **ConfgBUS** the system checks and classifies FE installed, and sets possible instructions for FE thus step-by-step creating the processing system by:

1. Making assignments of FE statuses for static and assignments of cycles for dynamic subsystems.
2. Provides tracing of communication for transfer of data and links FE.
3. Loads FE statuses to **ConfgBUS** and launches cycles.
4. Performs change of FE operation modes upon system instructions for each subsequent frame synchronous cycle.

• *Exclusive FE, used in the Adaptive System of 2D Processing and Visualization of image frames:*

1. **FVF (File-VideoFrame)** is FE for frames administration $\mathbf{Fr_{(i, j, k..)}}$ with open **H*V** format in double-buffer. Operates in in-sync mode with 16 bit matrix data input/output. Performs separate control of two data blocks (buffers) operating alternatively for data input or output, allows to ensure synchronous data flow at frame level, for frames with different delay in calculations in the conveyor. Performs asynchronous/synchronous control of both buffers within frame stream.
   Each buffer is a matrix of the image (i.e. instant data set) built on the basis of static memory - **SRAM** 16**M** pixel (**32MB**) with **H*V*16b** format.

2. **IN_LUT16 (Look Up Table)** is FE representing **LUT** for conversion of input/output data stream with functions defined and loaded by management system; features 2^{16} or 2^{17} values in each of the static tables. 4 tables **IN_LUT16 128k*16b** of static memory **SRAM** each are used in the conveyor processing.

- ***Elements of the conveyor indispensable for construction of digital systems stream 2D of processing and visualization, operating on a frames level.***

Performs functions of inter-frame manipulations, with simultaneous spectrum built-up of input intermediate frame, setting its maximum and minimum values per pixel:

- **FrPixNor –** pixel correction - a pixel from one frame is multiplied by an appropriate pixel from other frame, which represents a matrix of the same size loaded with correction coefficients for multiplying, with values range from 0 to to 1, and simultaneous summing of the third shift matrix:

  $\mathbf{Fr_k = Fr_i * Fr_c + Fr_s}$, где $\mathbf{Fr_c}$ – matrix of corrective coefficients for multiplying; $\mathbf{Fr_s}$ – shift matrix.

- **FrIntegr –** Add and accumulation of result (integration) down to full **16b** in a pixel:

  $\mathbf{Fr_k = Fr_{t1} + Fr_{t2} + \ldots + Fr_{tn}}$, where **n** – number of frames summed **1<n<=16**;

- **FrAddMx –** Cyclic add (up to 4 frames) - multiplying by average coefficients:

  $\mathbf{Fr_k = k_0 * Fr_{t0} + k_1 * Fr_{t-1} + k_2 * Fr_{t-2} + k_3 * Fr_{t-3}}$, где $\mathbf{0<=k_n<=1}$;

- **FrSubstr –** Cyclic between a frames subtraction:

  $\mathbf{Fr_k = Fr_g + Fr_i – Fr_j}$, где $\mathbf{Fr_g}$ - frame of an average grey field (permanent throughout the cycle) or specially created sequence of frames, **i** and **j** are two interdependent sequences of frames;

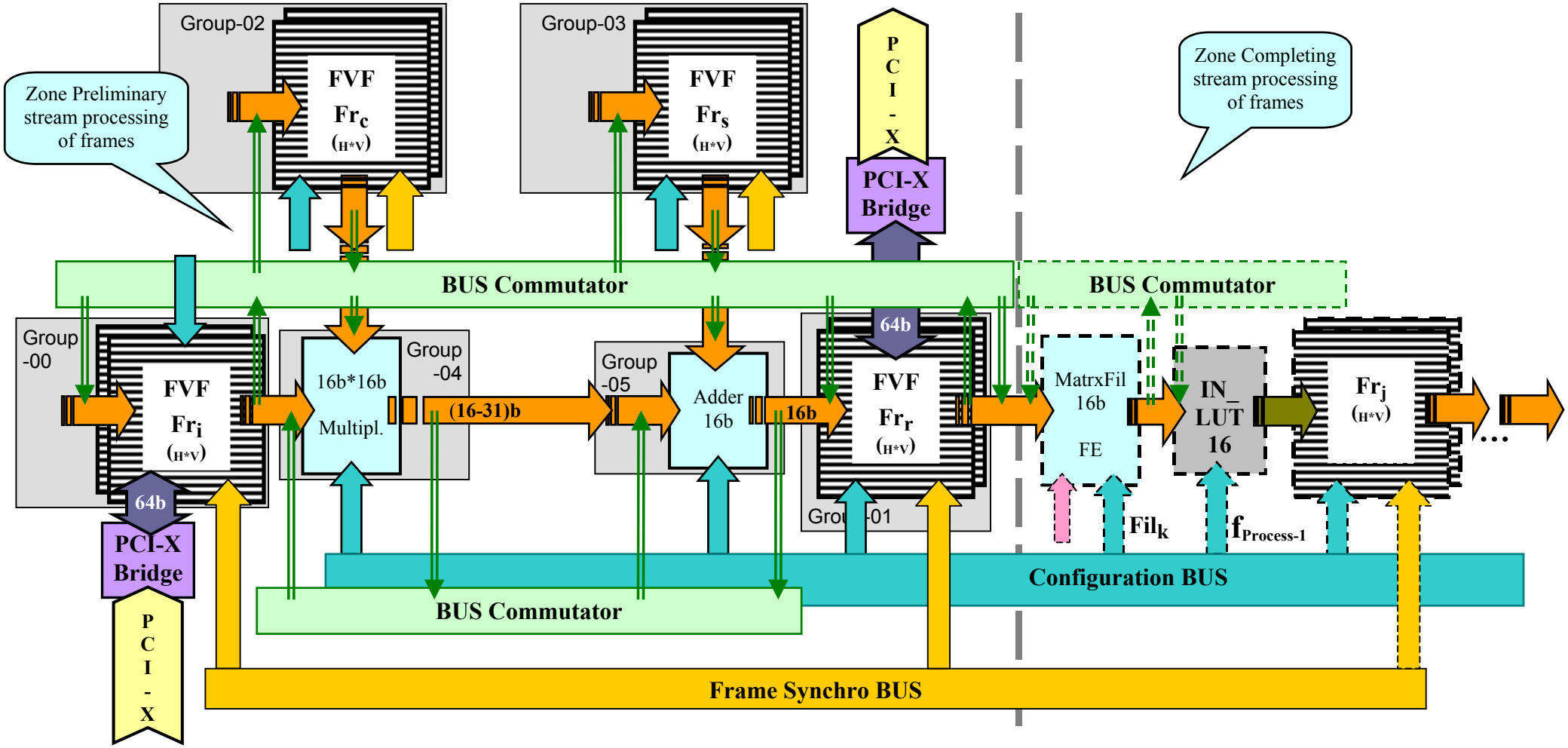
- Composite filters 3x3 matrix with padding mathematical manipulations computed only in a selected zone of frame:

  $\mathbf{Fr_k = ((Fr_i * Fil_{j1})^2 + (Fr_i * Fil_{j2})^2)^{1/2} * Fr_z}$, where
  $\mathbf{Fil_{j1}}$ и $\mathbf{Fil_{j2}}$ – matrix of integers, $\mathbf{Fr_z}$ – selected Zone, particular FE of a display image:

  – One-bit matrixes of integers representing the array in bits, equals to quantity of pixel in a frame, where the value of a pixel receives one of two values:
  =1 – shows that the given pixel is an element of selected zone,
  =0 – calculation for the given pixel is not performed.

- ***The Configuration of the architecture of the conveyor for stream correction of nonuniformity a pixel of display images.***

$$Fr_k = (f_{Process\text{-}1}\,(f_{Process\text{-}2}\,(*\ldots*\,(f_{Process\text{-}N}\,\{\,[\,(\,Fr_i * Fr_c\,) + Fr_s\,] * Fil_k\,\}))))),$$

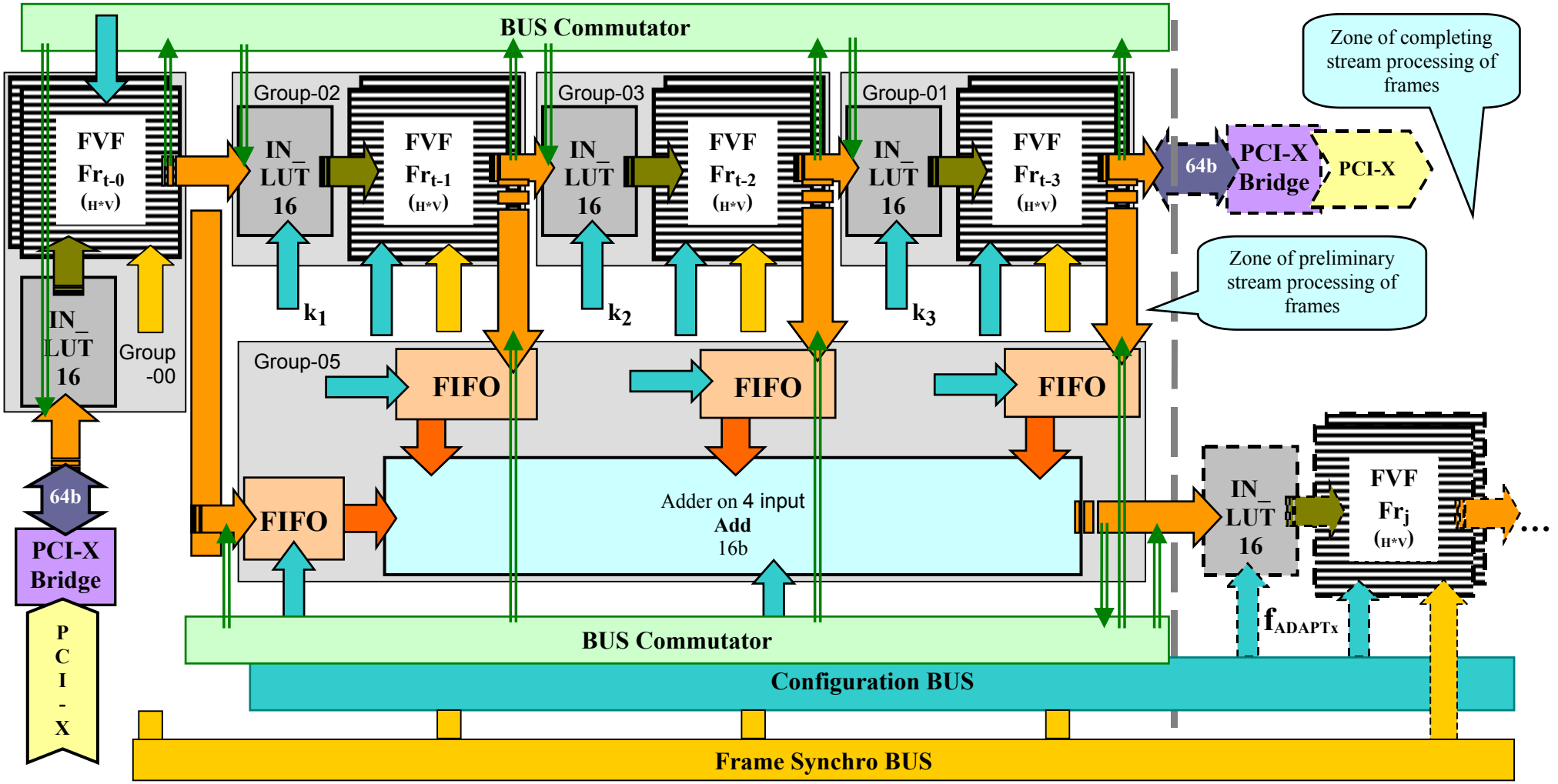


The matrixes FE **FVF** - Fr_c and FE **FVF** - Fr_s are static matrixes with multiplier and summator coefficients for each pixel of a frame, should necessarily have frame format.

The total delay in a zone of preliminary frame stream processing, by avoiding functional unit FE **FVF** - Fr_r, provides 2 frames, in view of recording the initial frames of the maps in FE **FVF** - Fr_i. On the circuit some are not rotined involved FE **IN_LUT16** from groups **IN_LUT16** and **FVF** (are switched on in operation FE **BUS_Commutator**).

- ***The configuration of the architecture of the conveyor for cyclic toting of frames at stream image processing.***

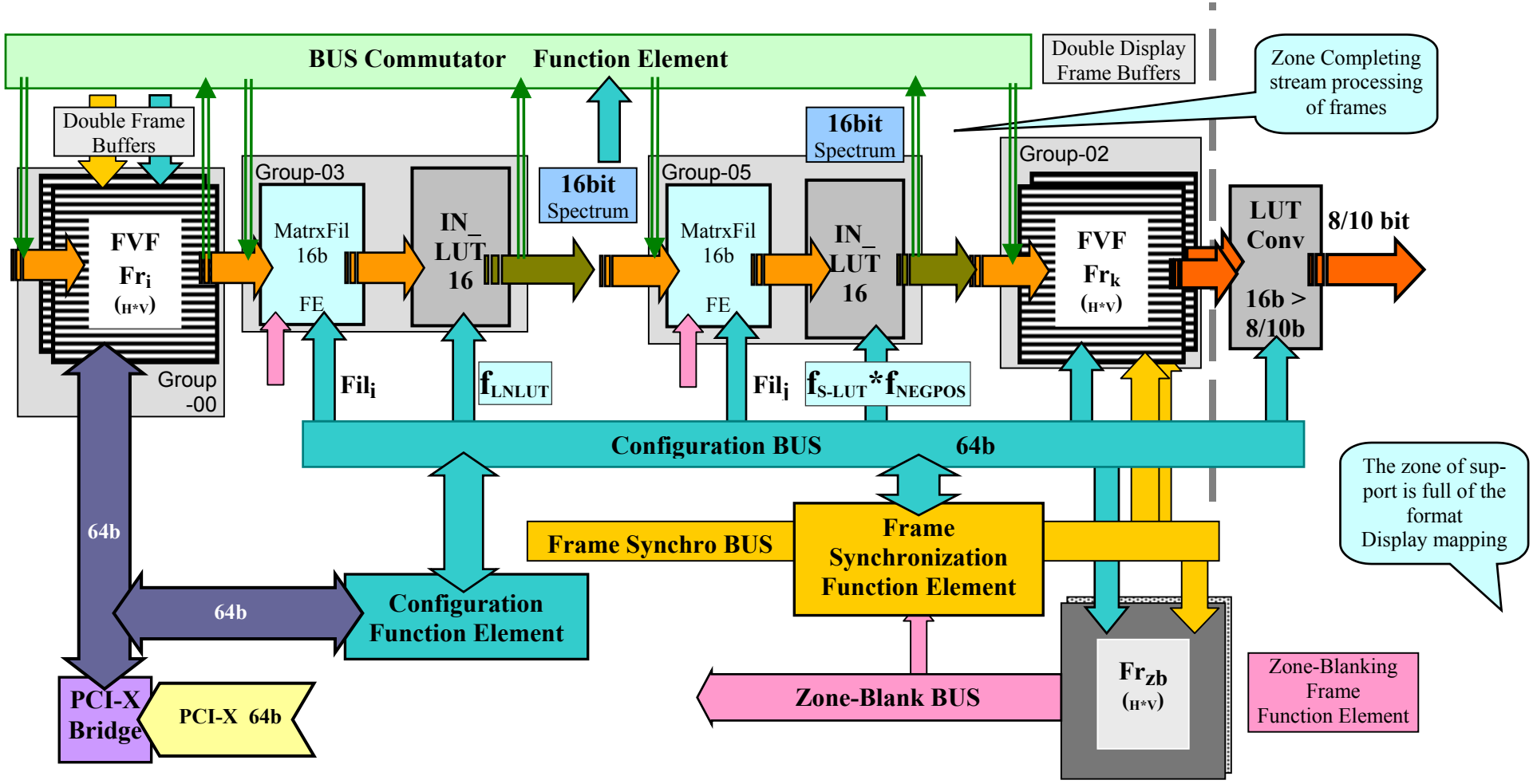
$Fr_k = k_0 * Fr_{t-0} + k_1 * Fr_{t-1} + k_2 * Fr_{t-2} + k_3 * Fr_{t-3}$, где $0 <= k_n <= 1$; $k_o = 1$. For example: $Fr_k = \ldots f_{ADAPTx} (1.0 * Fr_{t-0} + 0.5 * Fr_{t-1} + 0.25 * Fr_{t-2} + 0.125 * Fr_{t-3})$.



The total delay in a zone of preliminary frame stream processing, if bypassing FE Add_3, makes one frame, due to recording of the initial frames maps to FE **FVF** - Fr_{t-0}. Indexing **t-0 … t-3**, instead of **i, j, .. i**s applied for comprehension of conveyor operation the with stream of frames created in miscellaneous instants.

- ***The configuration of the architecture of the conveyor for filters at zonal stream image processing.***

$$Fr_k = f_{NEGPOS} \{ f_{S\text{-}LUT} [f_{LNLUT} (Fr_i * Fil_i * Fr_z)] * Fil_j * Fr_z \},$$

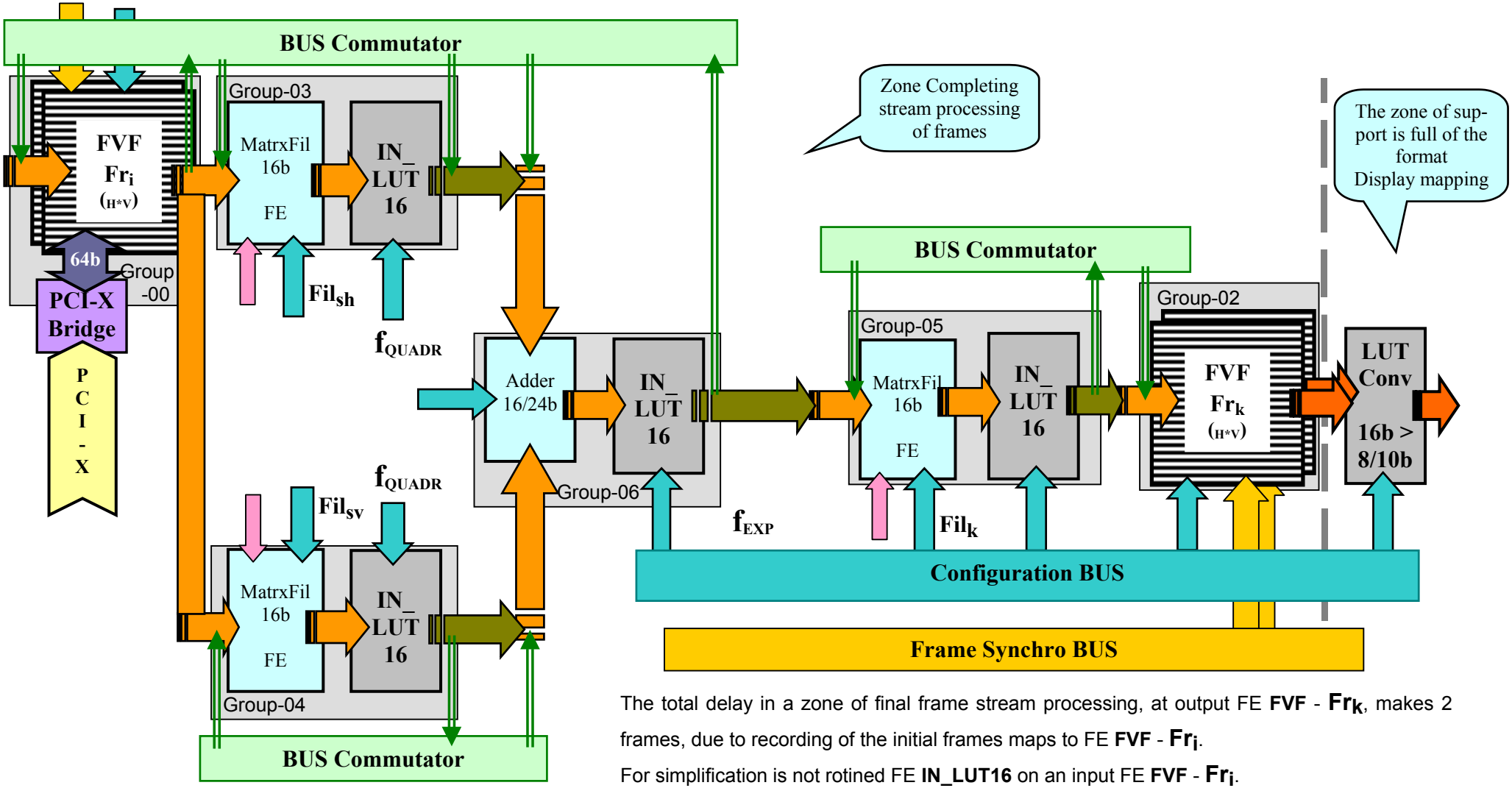


The total delay in a zone of final frame stream processing of, bypassing FE **FVF** - Fr_k, makes 2 frames, due to recording of the initial frames to FE **FVF** - Fr_i. For simplification is not rotined FE **IN_LUT16** on an input FE **FVF** - Fr_i.

- ***The configuration of the architecture of the conveyor for a composite function of zonal stream image processing.***

Implementation of a monogenic function of a filter - **Full Sobel**:

$$Fr_k = f_{ADAPTx} [(f_{EXP} \{ [f_{QUADR} (Fr_i * Fil_{sh} * Fr_z)] + [f_{QUADR} (Fr_i * Fil_{sv} * Fr_z)] \} * Fil_k * k_b) + Fr_i * (1- k_b)]$$

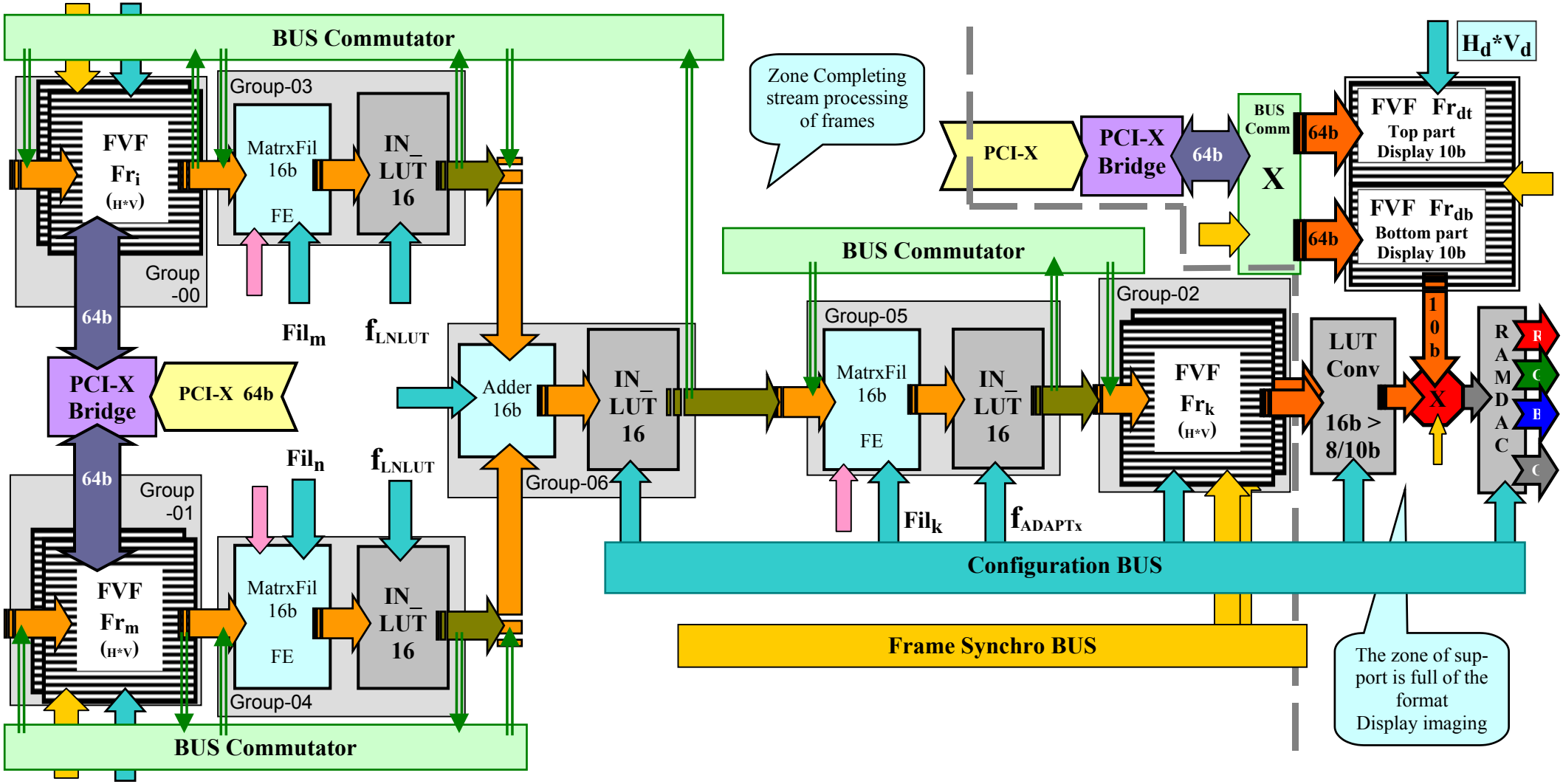


The total delay in a zone of final frame stream processing, at output FE **FVF** - Fr_k, makes 2 frames, due to recording of the initial frames maps to FE **FVF** - Fr_i.

For simplification is not rotined FE **IN_LUT16** on an input FE **FVF** - Fr_i.

- ***The configuration of the architecture of the conveyor for cyclic between frames zonal stream subtraction.***

$$Fr_k = f_{ADAPTx} (\{ [f_{LNLUT} (Fr_i * Fil_m * Fr_z)] - [f_{LNLUT} (Fr_j * Fil_n * Fr_z)] \} * Fil_k * Fr_z)$$



The total delay in a zone of final frame stream processing, bypassing FE **FVF** - Fr_k, makes 2 frames, due to recording of the initial frames maps to FE **FVF** - Fr_i and FE **FVF** - Fr_m. For sim-plification are not rotined FE **IN_LUT16** on inputs FE **FVF** - Fri and FE **FVF** - Fr_m.