Chips/Modules for **2D** Processing and Visualization. **Normalization.**

Systems 2D of Processing and the Visualization include 4 types of the chips/modules, that can be used separate (as an independent hardware products), or in any combination with each other: up to two or three modules together. Chips / Modules are being integrated according to the following subtypes:

1. Chips / Modules of normalization of graphic frames in real-time.
2. Chips / Modules for preliminary stream processing (normalization) of graphic frames in real-time.
3. Chips / Modules for final stream processing (post-processing) of graphic frames in real-time.
4. Chips / Modules for display mapping for graphics frames with high and super high resolution (HR).

Chips/Modules for stream processing (normalization) of HR graphics frames.

Stream Normalization of Frames is indispensable for technical systems operating with HR digital systems, and especially for those in real-time mode.

- The primary task for digital primary HR sensors of any type is alignment of non-uniformity of pixel sensitivity (normalization) across the whole image field. Is highly crucial for cases based on the image map assembly out of signals obtained simultaneously from several sensors – especially in a set of applied tasks. Such task are distinctive for digital HR systems operating without losses, where the simultaneous geometrically and physically heterogeneous radiant flux (light, X-ray etc.) hits the sensing unit.
- The secondary task for digital primary HR sensors of any type is improvement of a signal to noise ratio (S/N) achieved by manipulations with frame pixels, such operations as change of resolution, or inter-frame manipulations (timing). The possibility to operate with accumulated information over pixels/frames enables to receive better results if compared to direct physical data retrieval.
- The task of alignment non-uniformity of pixels across the whole field of HR frame is developed in screen monitors and projectors, where it is necessary to linearize (to normalize) non-uniformity of a thermal radiation for each pixel of a display device, especially in poly-monitors or poly-screen applications.

The task of real-time normalization of pixel for a continuous flow of data at the frequency 25-30 frame/sec and **1k*1k** format has not been resolved by any corporation as of today. And real-time pixel normalization for frames with even higher resolution has become a vital demand.

The absence of normalization affects image processing first of all results in worse S/N ratio, and appearance of numerous artifacts (noise) on the picture itself. In cases with pixel normalization the pixel it becomes possible to increase the accuracy sensor output signals thus allowing the use of sensors with milder tolerance to parameters, therefore cheaper ones. The only requirement for source signal becomes linearity of the function at the stage of converting each pixel from input signal.

Same problem of pixel normalization persists for static HR images from **2k*2k** and higher.

The only exception makes computer thomograph[1] (**CT** Scanning System), where re-calculation of pixel non-uniformity coming from sensors is carried out at apparatus workstation, otherwise it becomes impossible to obtain the image map due to of substantial non-uniformity of raw data coming from both internal set of x-ray detectors, as well as between the sensor sets. The task is solved by post-processing methods rather than by real-time electronics engineering.

Douglas R. Dykaar and G. Luckhurst in their work «Chromatic Aberration and Color Balancing Issues with Common Optical Axis CCD Cameras» (www.dalsa.com) in section 4 - «Color balancing issues» suggest to solve this problem even with **DSP** processors appearing frame capturing boards!

What we offer

To achieve implementation of the process of normalization a pixel in a real-time mode we suggest to use chip(s) built by the philosophy called «**Adaptive Systems for 2D Processing and Visualization**».

The chip technology for pixel normalization is similar of the above mentioned in section 4 of this paper. The matrixes of coefficients are calculated for each sensor individually taking into account all factors influencing the modules. It is either the detector itself that is being normalized, or the entire path **Emitter – Converters – Sensor – Digit** that is even more efficient.

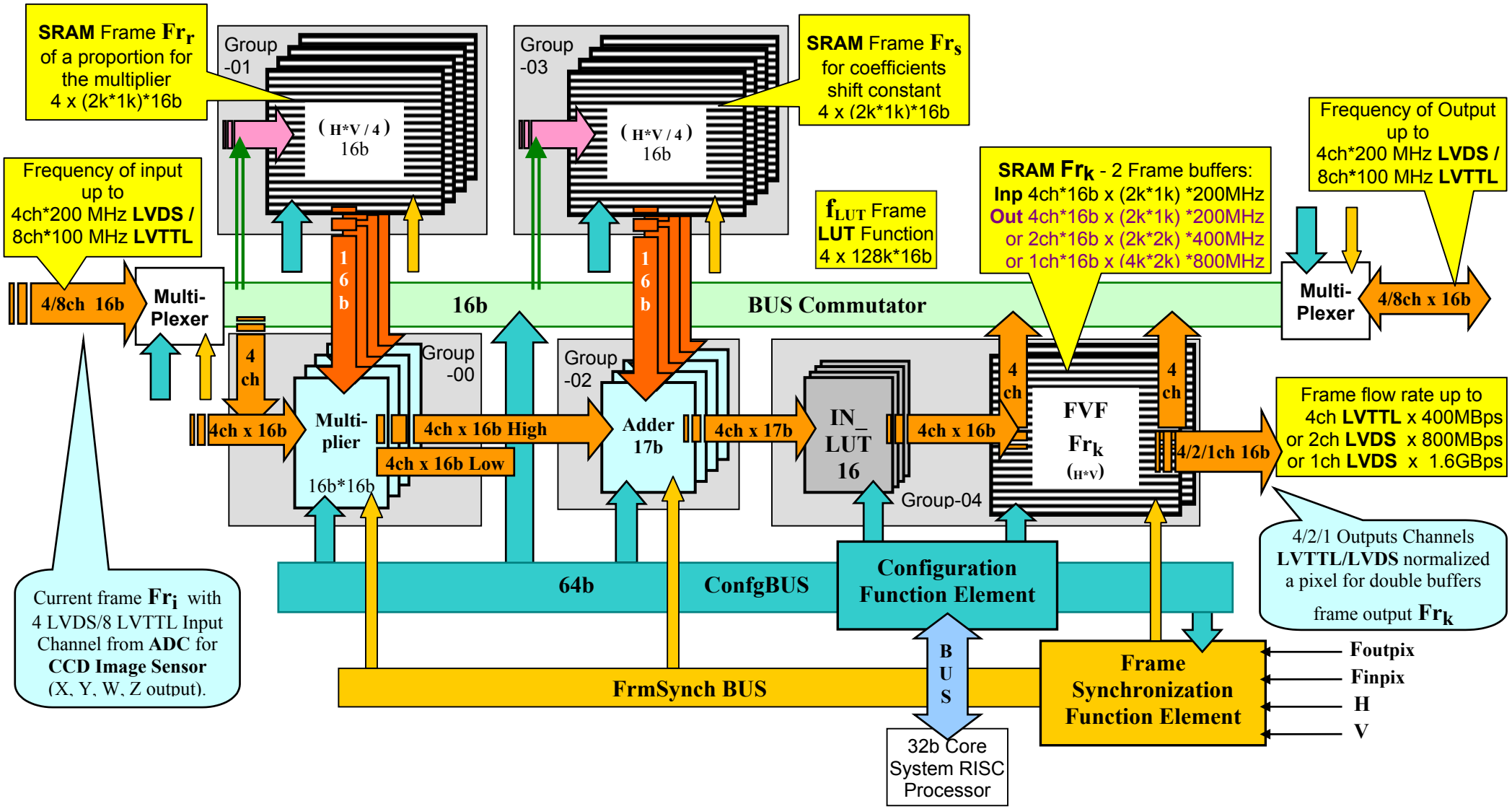
The chip described above is a part of more General program aimed to build up the chip conveyor for ***2D Processing and Visualization*** of HR images in real-time mode.

[1] (by demand for computing processes known as «restoring of images on projections».

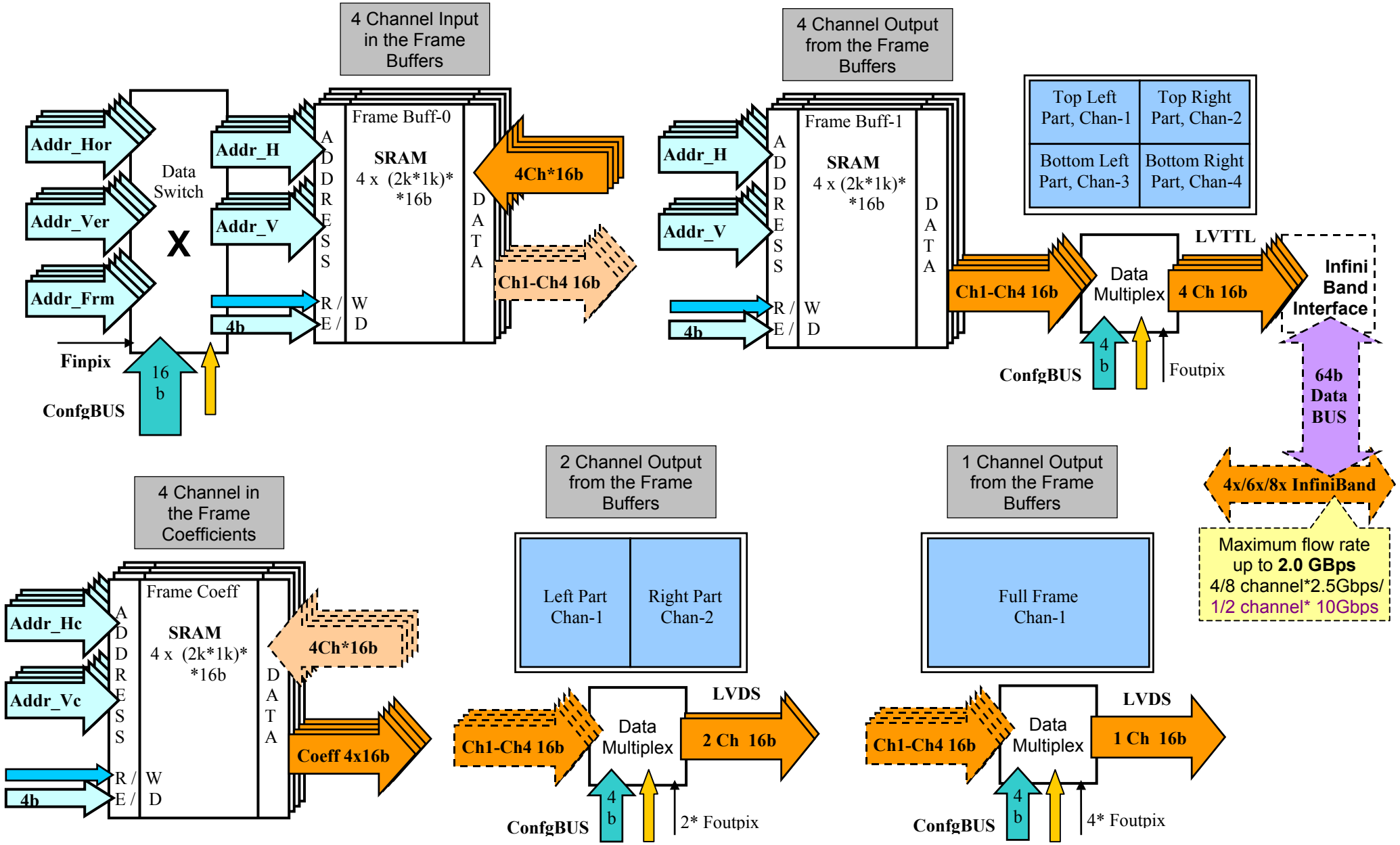
The architecture of the conveyor of stream correction of non-uniformity (normalization) a pixel.

All path of datas - 4 channel and completely 16 bit, frequency of input / data output up to 200MHz!!

$Fr_k = \{ f_{LUT} [(Fr_i * Fr_r) + Fr_s] \}$. The matrixes FE Fr_c and Fr_s are static matrixes of coefficients of the multipliers and summators for each pixel of a frame.



The architecture of handle of parts FE FVF - one of control channels (phase A and B).



Technical parameters

4-channel buffers of aspect ratios **Fr_r**, represent simplified FE **FVF** with static memory **2k*1k*16b** on each channel. Is adapted for line/frame synchronization with freely set initial and output parameters for both lines and frames.

4-channel buffers of coefficients of shift **Fr_s**, represent simplified FE **FVF** with static memory **2k*1k*16b** on each channel. Is adapted for line/frame synchronization with deliberately set initial and output parameters for both lines and frames.

4-channel FE the multiplier **Multiplier 16b*16b**, works on synchronous frequency of data entry as the result of synchronous multiplying of each multiplier shifted by clock tick.

4-channel FE the summator **Adder 17b** - input two streams synchronous **16b** data at input, and **17b** data at output with shift by clock tick.

4 FE **IN_LUT16** – with uploaded programmed functions to convert **17b** input data to an output **16b** data. **IN_LUT16** represents static synchronous memory with **128k*16b** for each channel. FE **IN_LUT16** allows to apply any gamma, logarithmic, S-shaped or other conversion functions to change spectrum of output data according to the tasks of the operator. Mode of operation is synchronous, with shift by clock tick.

FE **FVF** of frame buffers for parallel data acquisition from 4 FE **IN_LUT16** with the subsequent conversion of the frame (or its elements) format and, accordingly, output channels depending on output frame format. The maximum size of the frame buffer is **4x (2k*1k*16b)**, that allows to load one **4k*2k*16b** frame, and for frames with smaller sizes (aliquot to 2) the following sizes **2k*2k*16b**, **2k*1k*16b** and **1k*1k*16b** into each of frame buffers (**2, 4, 8** frames accordingly). The buffers alternately vary by functions: either upload or download of frame segments or the entire frame(s).

FE **BUS Commutator** paired to the system bus of processor that controls loading of matrix coefficients and values from **LUT** tables. There are four/eight channel **16b** multiplexers – **Multiplexer** for input/output of frames on lines **LVDS/LVTTL** and there are four-channel **16b** link buses to FE **Multiplier**, with FE **FVF** buffer for twin output of frames.

Field synchronization bus – FE **FrmSynch BUS** – synchronizes operation performed by coefficients buffers equipped with CCD Image Sensors or processing alternative data streams.

Configuration and management bus – FE **ConfgBUS** – represents itself specialized control 64 bit bus.

Options: Integration options include four/eight channel **2.5Gbps/channel** or one/two channel **10Gbps/channel** serial interface **InfiniBand** for fast-track output of frames.

Examples of application

(Samples of application of preliminary stream processing of frames aimed to rectify non-linearity of primary sources)

1. Digital Cine Cameras **ORIGIN** with **4k*2k/24fps** format, designed for digital cinematography consisting of 4 **2k*1k** matrixes and 4 parallel channels for output of digitized **14b** data. Formation of uniformity between pixels in both CCD matrixes itself as well as between CCD matrixes, different colors, in parallel streams. Formation of intensity uniformity of a film at digitization of movies, correcting either the whole frame, or in-between frames of same part of movie with simultaneous RGB gamma correction.
2. Digital **2k*2k 30fps** cameras, featuring 4 matrix **1k*1k** sets with four parallel output channels at **12b*40MHz**. The correction of non-uniformity between pixels in parallel streams is especially required in medical roentgenology at **DSA** (Digital Subtraction Angiography) regimes
3. Digital **1k*1k 30/60/75/150fps** cameras, using 2 /4 parallel output **12b*40/60/100/150MHz** channels. Correction of non-uniformity between pixels in parallel streams, especially for applications in a medical roentgenology at rapid digital filming.
4. Projectors in Digital Cinematography – correction of non-uniformity of light balance by each pixel on the whole screen for each color separately, as well as between projectors working in poly-screen systems. Same is applicable for **HDTV** projectors though to a smaller degree subject to inhomogeneous mapping, but the need for solutions is there.
5. Systems of output of HR **2k** (and higher) to screen monitors for systems with color calibration of complete image map.
6. Medical computer tomographers (CT) feature essential non-uniformity of raw data from x-ray detectors, both between sets of sensors and inside one set. The solution is in electronics engineering.
7. Roentgenology features digital Flat panels up to **4k*4k** and larger with the size 430*430мм, where the alignment of pixel non-uniformity caused by geometrical discrepancies needs to be solved, additionally the task to minimize time of calculation to facilitate rapid filming operation required by medical technologies, based on in-between manipulations with frames.
8. In systems serving to correct pixel non-uniformity, at stage of image alignment, caused by non-uniformity of radiation from the source. To be adjusted by re-calculation of the entire data flow route: *Source Radiation - Converters – Detector – ADC – Correction Output*.